IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A method for analyzing defects in electronic circuit patterns, comprising: ~~the following steps:~~

a step for ~~detecting a defect in an inspected~~inspecting a first object ~~and storing position information for said detected defect~~to detect defects during a production process and obtaining position information of said defects;

a step for ~~collecting detailed information~~detecting images of said ~~defect~~ defects ~~for which~~using said position information of said defects obtained ~~is stored and storing said collected detailed information in association with said defect position information~~;

a step for ~~electronically testing~~performing an electronic test on said ~~inspected~~ first object ~~and storing~~ after said production process is completed to detect faults in said first object and obtain position information ~~for a position at which a fault is generated in said electronic test~~of said faults;

a step for comparing said ~~stored defect~~position information ~~and said fault generating~~ of said defects with said position information of said faults and extracting defects having common position information between said defects and said faults;

a step for classifying ~~said detected defect based on results from said comparing step~~images of extracted defects into critical defect images and non-critical defect images based on a classification rule; ~~and~~

a step for displaying ~~information relating to said~~ images of classified ~~defect.~~ defects on a screen by discriminating between said critical defect images and said non-critical defect images;

a step for modifying said classification rule by correcting classification of classified defect images displayed on the screen;

a step for inspecting a second object during the production process to detect defects and obtain information of said defects including position information and image of said defects;

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a step for classifying images of said defects detected on said second object into critical defects and non-critical defects by using a modified classification rule; and

a step for outputting information on said classified defect images of said second object.

Claims 2-4 (Canceled):

Claim 5 (Currently Amended): A method for analyzing defects in electronic circuit patterns comprising; ~~the following steps:~~

a step for inspecting a first ~~inspected~~ object to detect defects during a production process and obtaining information relating to said defects on the first object including position information and detailed information, and storing information relating to ~~a defect detected by said inspection including~~ said position information ~~of said~~and detailed information of ~~detected defect~~said defects;

a step for performing an electronic test on said first ~~inspected~~ object after said production process is completed to detect electronic faults in said first ~~inspected~~ object and obtain position information of said electronic faults and storing ~~fault generation position information~~said position information of said electronic faults;

a step for comparing ~~said~~ stored position information of said ~~defect detected in said inspection of said first inspected object during said production process with said electronic test fault generating position detected by said electronic test performed on said first inspected object after said production process is completed~~defects with stored position information of said electronic faults and classifying said stored position information of said defects into critical defects and non-critical defects;

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a step for classifying ~~said detected defect during said production process based on said comparison result~~stored detailed information of said defects into critical defects and non-critical defects under a classification rule referring to classified position information of said defects; ~~and~~

a step for modifying said classification rule by correcting classified detailed information;

a step for inspecting a second object during the production process to detect defects and obtain position information and detailed information of said defects on the second object;

a step for classifying said detailed information of said defects on the second object into critical defects and non-critical defects using a modified classification rule; and

a step for outputting information on ~~said~~ classified ~~defect~~defects.

Claim 6 (Canceled):

Claim 7 (Currently Amended): A method ~~for analyzing defects in electronic circuit patterns as described in claim 6~~as claimed in claim 5, wherein, in the step for classifying said detailed information of said defects on the second object, said non-critical defects ~~in said detected defects~~ are further classified into at least two categories.

Claim 8 (Currently Amended): A method ~~for analyzing defects in electronic circuit patterns as described~~as claimed in claim 5, wherein ~~information relating to a fault~~in the step for outputting, defect generation rate for each ~~classification of said classified defects is output~~defect class classified in the step for classifying said obtained detailed information of said second object is outputted.

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Claims 9-11 (Canceled):

Claim 12 (Currently Amended): A method ~~for analyzing defects in electronic circuit patterns as described~~as claimed in claim 5, wherein said ~~detected defect images are displayed by classification as said classified defect information~~detailed information is a defect image.

Claim 13 (Currently Amended): A method for analyzing defects in electronic circuit patterns comprising: ~~the following steps:~~

a step for inspecting a first ~~inspected~~ object during a production process ~~and detecting defects~~to detect defects;

a step for obtaining information ~~relating to~~of said ~~detected~~ defects including ~~defect~~ position information of said defects;

a step for performing an electronic test on said first ~~inspected~~ object after said production process has been completed ~~and detecting~~to detect electronic testing faults in said first ~~inspected~~ object;

a step for obtaining position information on said ~~detected~~ electronic testing ~~fault generating positions~~faults;

a step for comparing ~~said~~ obtained ~~defect~~ position information ~~and said electronic testing fault generating positions and extracting defects for which both position informations match or are close to matching~~of said defects with obtained position information of said electronic testing faults and extracting defects having common position information between said defects and said electronic testing faults;

a step for classifying ~~said~~ extracted defects into critical defects and non-critical defects ~~and~~ based on a classification rule;

a step for displaying ~~said defects on a screen~~classified defects on a screen by discriminating between said critical defects and said non-critical defects; ~~and~~

a step for modifying ~~classifications of said defects displayed on said screen~~said classification rule by correcting a classified result of said defects displayed on the screen;

a step for inspecting a second object during the production process to detect defects and obtain information of said defects including position of said defects;

a step for classifying said defects detected on said second object into critical defects and non-critical defects by using said modified classification rule; and

a step for outputting information on classified defects on said second object.

Claims 14-15 (Canceled):

Claim 16 (Currently Amended): A system for analyzing defects in electronic circuit patterns comprising:

a first memory which stores position information ~~of defects~~and detailed information of individual defects detected ~~by a detection of an~~on a first object during a production process;

a second memory which stores ~~detailed~~ position information of ~~said defects, which is obtained through an inspection using said position information stored by said first memory means, in association with said position information of said~~electronic testing faults detected on said first object with an electronic test after said production process has been completed;

~~a third memory which stores a position information of electrical defects detected by a electrical testing;~~

a ~~comparater~~ comparator which compares said position information of said defects stored in said ~~second~~ first memory ~~and said~~with said position information of electrical ~~defects~~ testing faults stored in said ~~third~~ second memory;

~~a~~ first classifying means for classifying said ~~detailed~~ position information ~~stored in said second storing means based on comparison results from said~~

~~comparater~~of said defects either critical defects or non-critical defects using a first classification rule; ~~and~~

second classifying means for classifying said detailed information of said defects either critical defects or non-critical defects referring to classified position information of defects using a second classification rule;

modifying means for modifying said second classification rule by correcting classified detailed information classified by said second classification means;

a third memory for storing both position information and detailed information obtained from a second object during the production process;

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third classifying means for classifying said detailed information of defects detected on said second object either critical defects or non-critical defects using a modified second classification rule; and

~~an~~ outputting means which ~~output~~ outputs information ~~relating to said detailed information~~of defects classified by said third classifying means.

Claims 17-18 (Canceled):

Claim 19 (Original): A system ~~for analyzing defects in electronic circuit patterns as described~~as claimed in claim 16, wherein said second classifying means ~~classifies said non-critical defect images further into at least two categories~~subdivides at least one of said detailed information of critical defects and that of non-critical defects referring to those similarity before teaching said third classifying means.

Claims 20-22 (Canceled):

Claim 23 (Currently Amended): A system for analyzing defects in electronic circuit patterns comprising:

~~first storing means for storing~~a first memory which stores position information ~~of defects detected through an inspection of a object~~and detailed information of individual defects detected on a first object during a production process;

~~second storing means for storing an image of said defects, which is observed using said position information stored by said first storing means, in association with said position information of said defects;~~

a ~~third~~ second memory which stores [[a]]position information of ~~electrical defects~~electrical testing faults detected ~~by a electrical testing~~on said first object by an electronic test after said production process has been completed;

a comparator which compares said position information of said defects stored in said first memory with said position information of said electrical testing faults stored in said second memory;

first classifying means for classifying said ~~defect images stored in said second storing means using said defect images stored by said second storing means and electronic test fault generating position information stored by said third storing means~~position information of said defects either critical defects or non-critical defects by using a first classification rule; ~~and~~

second classifying means for classifying said detailed information of said defects either critical defects or non-critical defects referring to classified position information of said defects by using a second classification rule;

display means for displaying said defects classified by said second classifying means on a screen;

modifying means for modifying said second classification rule by correcting classified detailed information classified by said second classification means and displayed on the screen; and

outputting means ~~for outputting~~which outputs information ~~relating to said~~of defects classified by said second classifying means using a modified second classification rule.

Claim 24 (Currently Amended): A system ~~for analyzing defects in electronic circuit patterns as described~~as claimed in claim 23, wherein said ~~classifying means classifies said defect images into critical defect images and non-critical~~ detailed information is a defect ~~images~~image.

Claims 25-28 (Canceled):

Claim 29 (New): A system as claimed in claim 23, wherein said outputting means outputs a defect image as said detailed information of defects to said display means, and said display means displays the defect image classified by said second classifying means using said modified second classification rule.

Claim 30 (New): A method as claimed in claim 5, further comprising:

a step for counting number of the defects classified as critical defects at the step for classifying said detailed information of defects on said second object; and

a step for displaying information of a counted number of said defects classified as critical defects.

Claim 31 (New): A method as claimed in claim 13, wherein, in the step for classifying said detailed information of defects on said second object, said non-critical defects are further classified into at least two categories.

Claim 32 (New): A method as claimed in claim 13, wherein, in the step for outputting, a defect generation rate for each defect class classified in the step for classifying said detailed information of defects on said second object is outputted.